Figure 1: Self Addressing Microlocations (Microlithographic Fabrication)

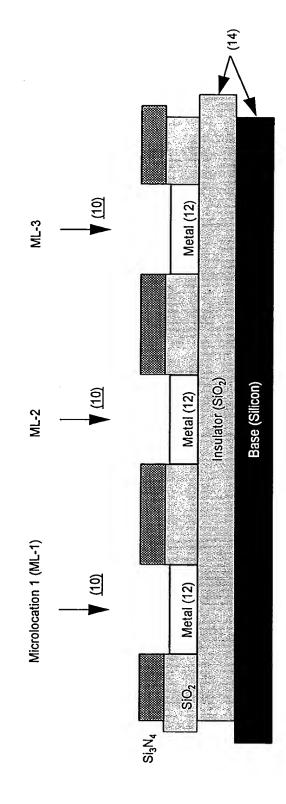


Figure 2: Microlocation Design Features

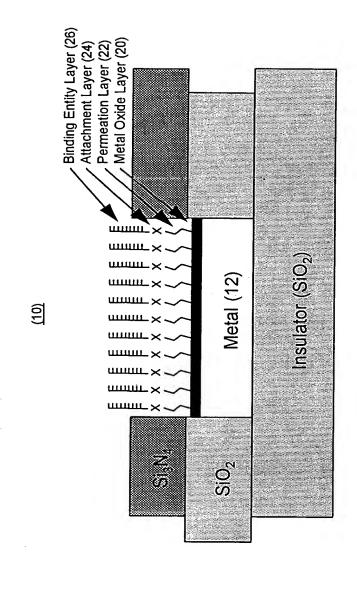
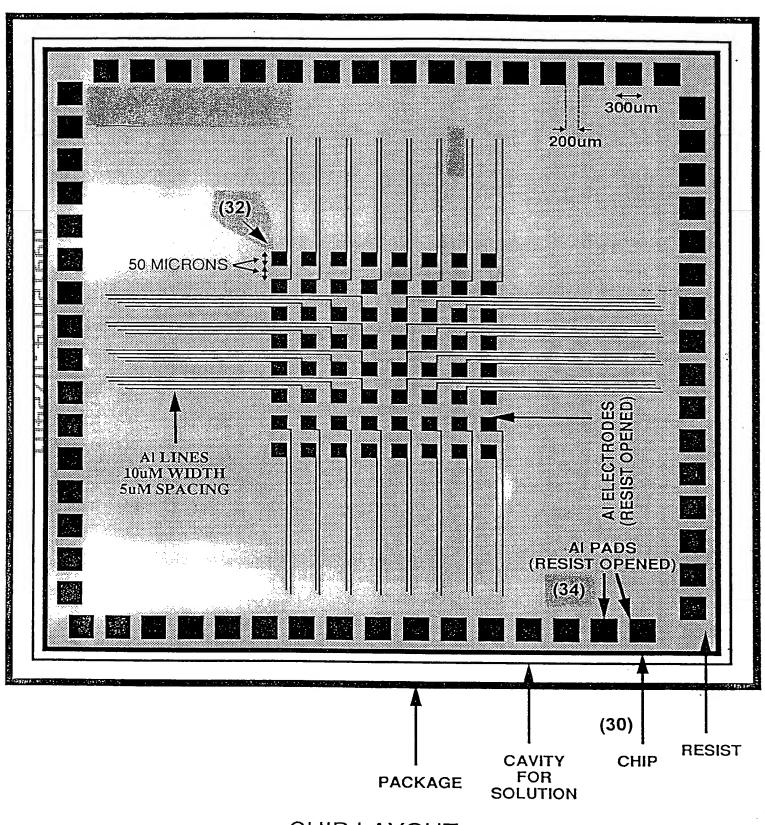


Figure 3: Self-Addressable 64 Microlocation Chip



CHIP LAYOUT

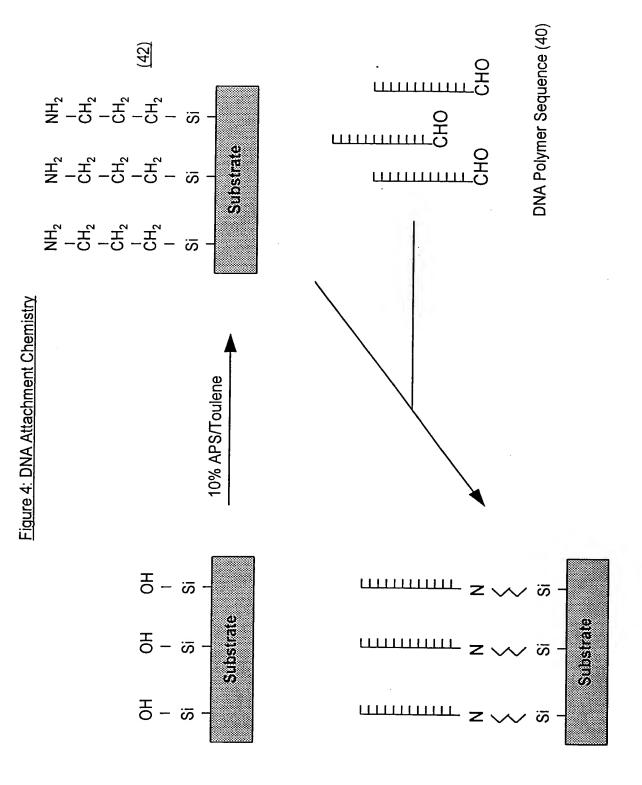


Figure 5: Micro-Machined Device (Exploded View)

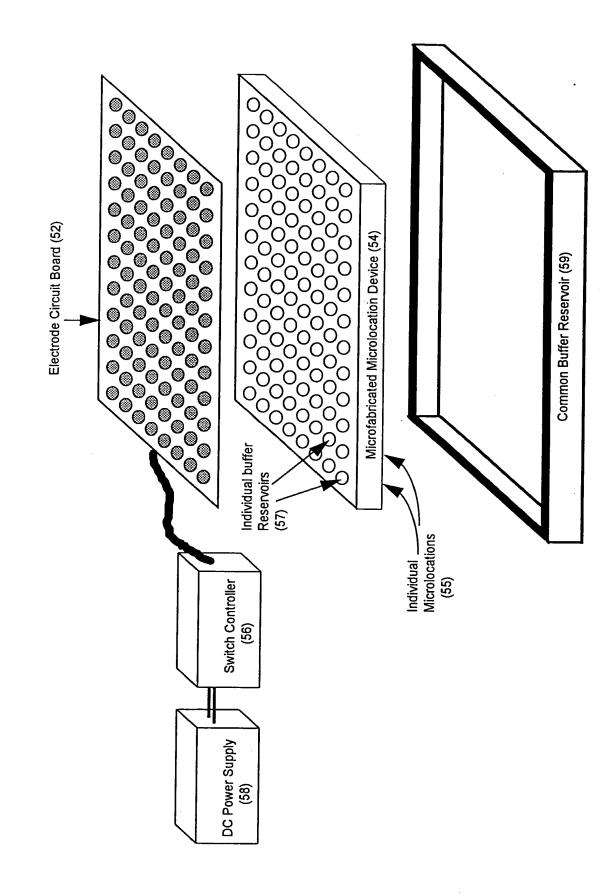
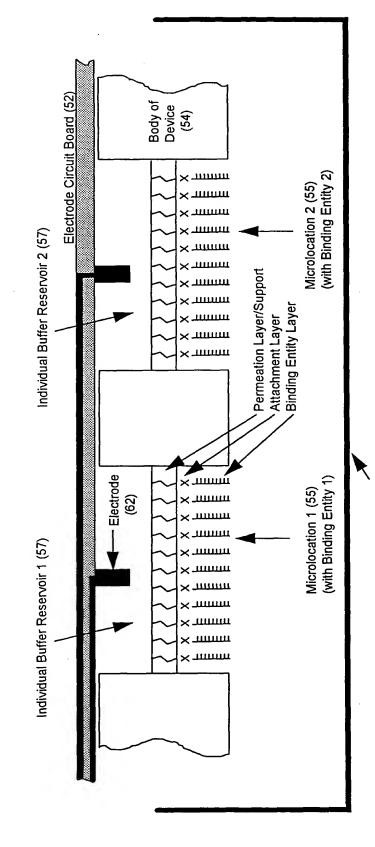
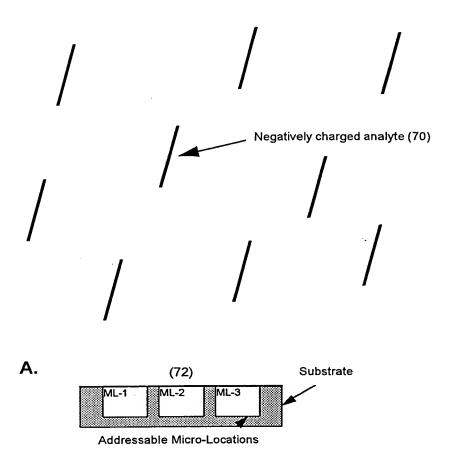


Figure 6: Micro-Machined Device (Cross-Section)



Common Buffer Reservoir (59)

Figure 7: Electronically Controlled Concentration Effect



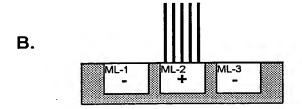


Figure 8: Electronic Addressing and Self-Directed Assembly of Device.

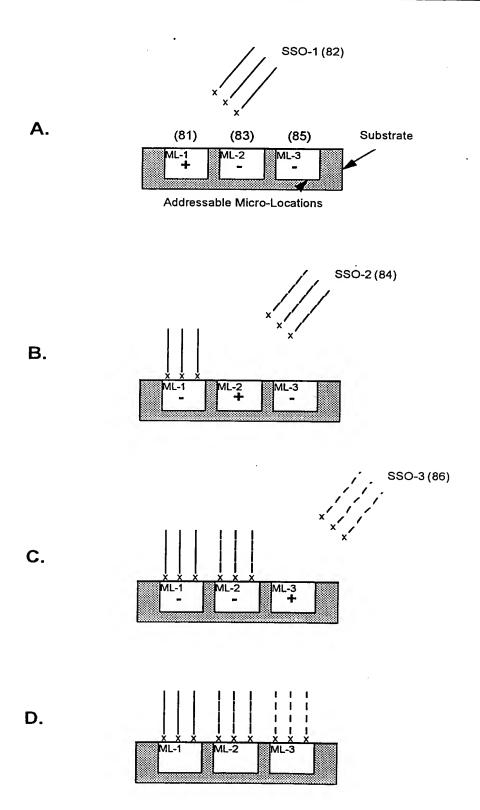


Figure 9: Electronically Controlled Hybridization Process

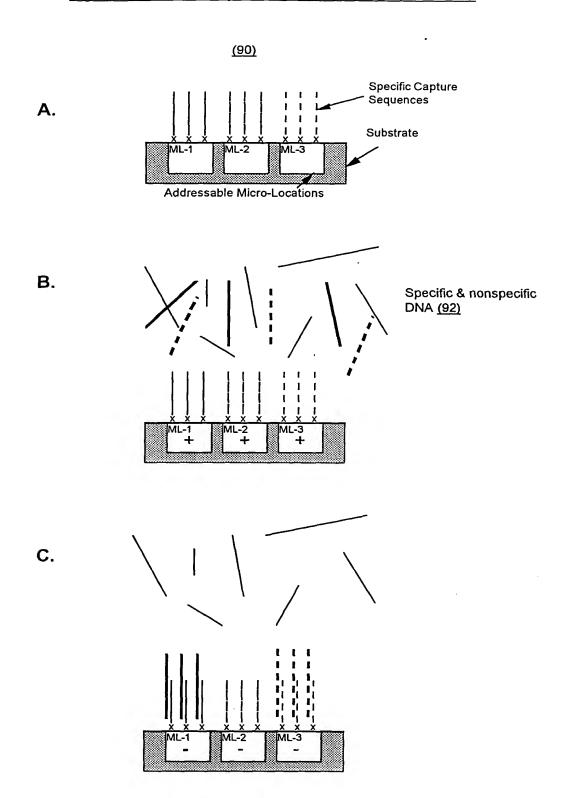


Figure 10: Electronically Directed Serial Hybridization Process

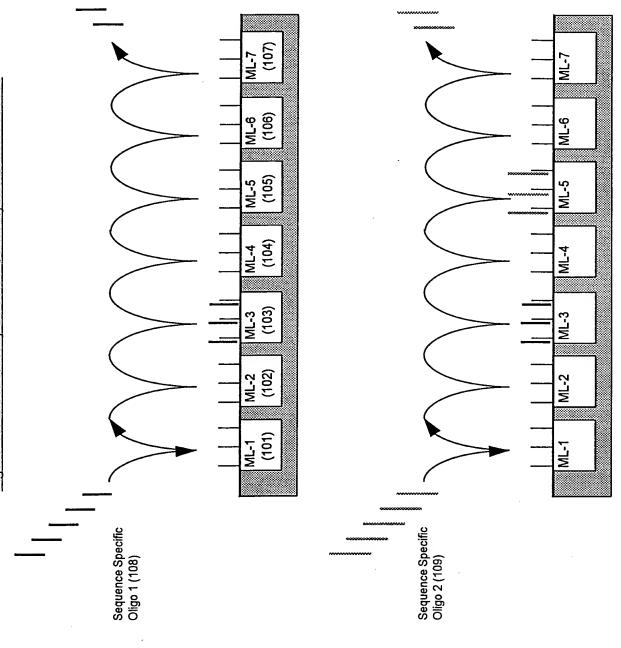
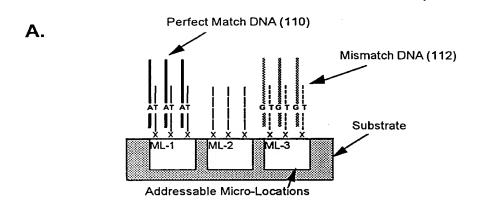
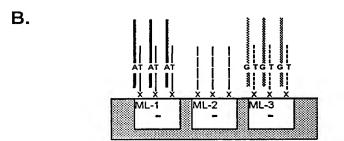


Figure 11: Electronic Stringency Control (ESC) of Hybridization Process





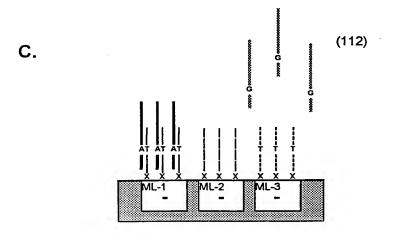


Figure 12: Electronically Controlled Fluorescent Dye Detection Process

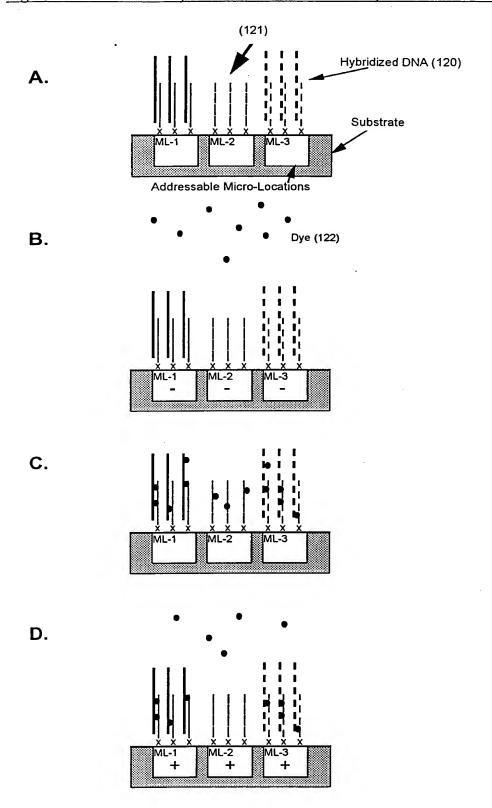
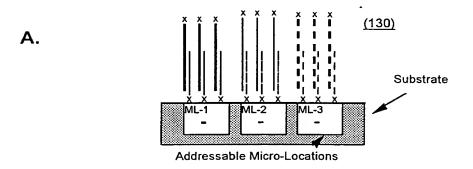
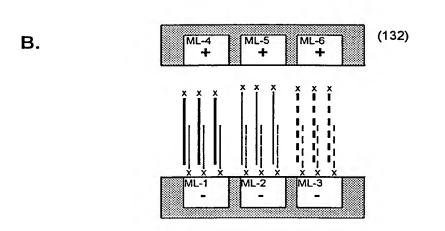


Figure 13: Electronically Controlled Template Replication





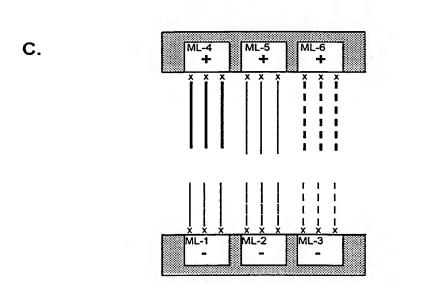


Figure 14: Electronically Directed Combinatorial Synthesis.

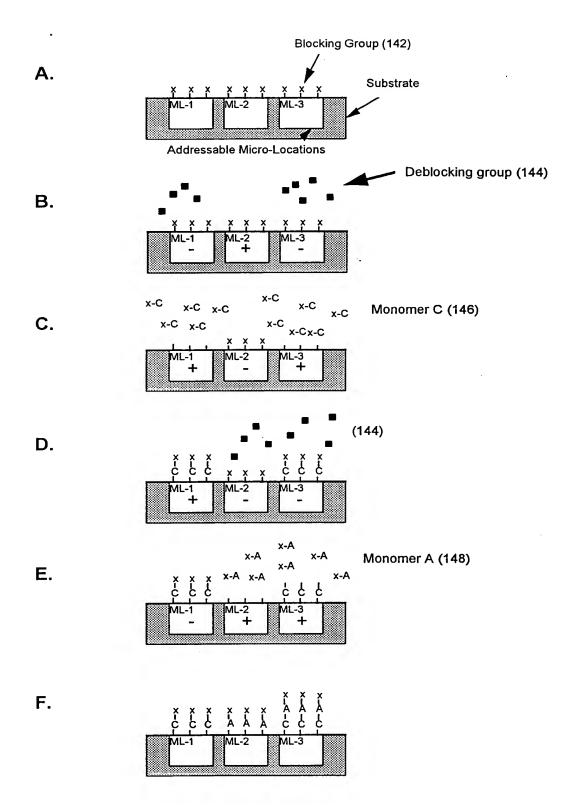


Figure 15. Tolt bed

Relative Sensitivity for Mismatch Discrimination

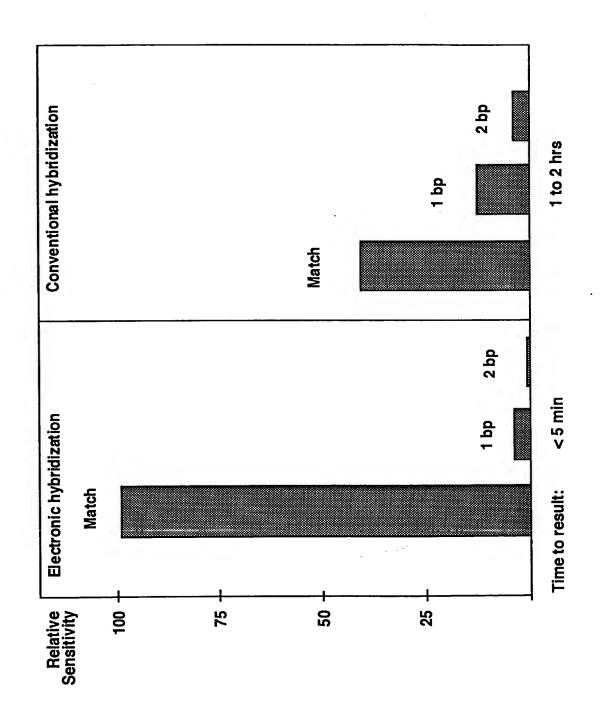


Figure 16
Electronic Restriction Cleavage

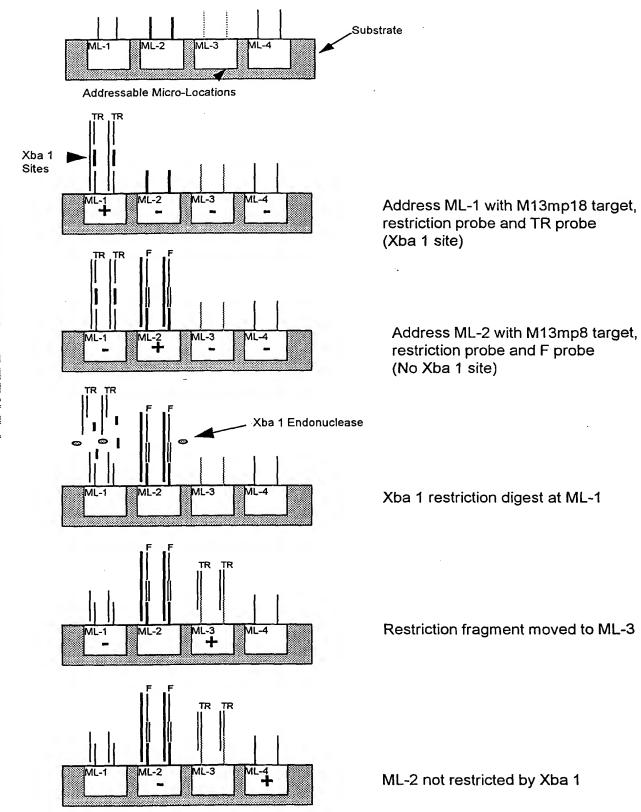


Figure 17

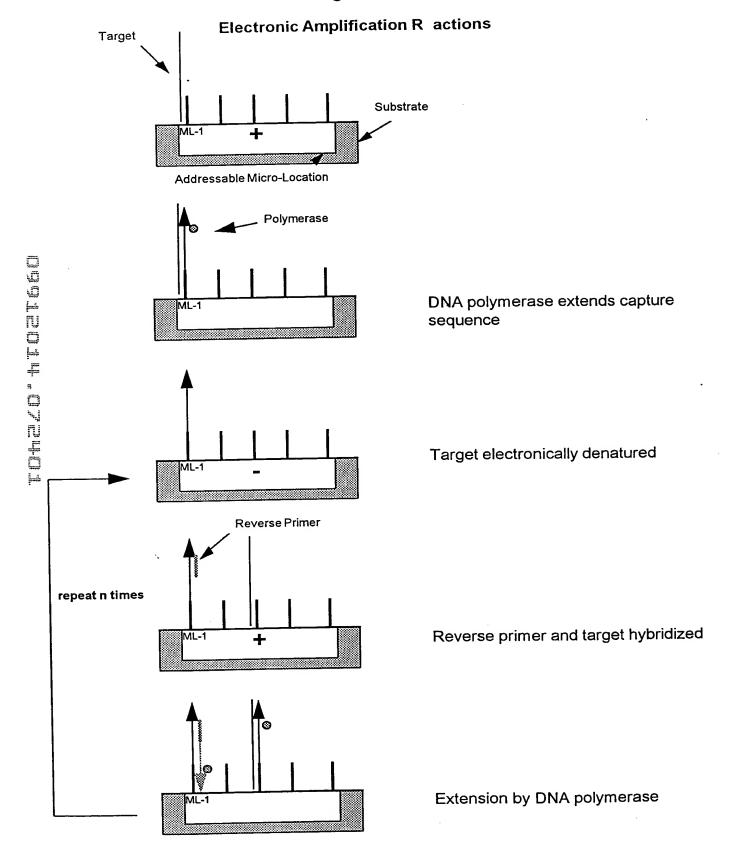


Figure 18

Complete APEX System with Sample Preparation

